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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER

O BRIEN, BARRY J

ART UNIT	PAPER NUMBER
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2183

DATE MAILED: 04/07/2004

4

Please find below and/or attached an Office communication concerning this application or proceeding.

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Office Action Summary

Application No.

09/838,461

Applicant(s)

EICKEMEYER ET AL.

Examiner

Barry J. O'Brien

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 4/19/01, 8/6/01 and 8/13/01.
2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-19 is/are pending in the application.
4a) Of the above claim(s) _____ is/are withdrawn from consideration.
5) ☐ Claim(s) _____ is/are allowed.
6) ☒ Claim(s) 1-19 is/are rejected.
7) ☐ Claim(s) _____ is/are objected to.
8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date 3.
4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-19 have been examined.

Papers Submitted

2. It is hereby acknowledged that the following papers have been received and placed on record in the file: Letter from Draftsman as received on 8/6/2001 and IDS as received on 8/13/2001.

Specification

3. The lengthy specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.
4. The applicant is requested to review the specification and update the status of all co-pending applications made mention of, replacing attorney docket numbers with current U.S. application or patent numbers when appropriate.

Claim Objections

5. Claims 14 and 17 are objected to because of the following informalities:
 - a. Claim 14 recites the limitation, "the plurality hold state latches" on line 3 on p.19 of the instant application. Please correct the claim language to read, "the plurality of hold state latches" to read more clearly. Please see a similar problem in claim 17.

Appropriate correction is required.

Claim Rejections - 35 USC § 112

6. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

7. Claims 1, 4, 7, 10, 13 and 17 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

8. Regarding claim 1, the limitation, “the thread control unit provides a thread control signal to said hold latches and registers selecting a thread using said data” on lines 12-14 on p.16 of the instant application. It is unclear whether the latches and registers select the thread, or whether the control signal selects the thread. Please correct the claim language to more clearly point out the metes and bounds of this claim language. For the purposes of this examination, the examiner will assume that the thread control signal, which is sent to the latches and registers, selects the thread. See also similar problems in claims 7 and 13.

9. Regarding claim 4, the limitation, “the thread control unit returns said hold latches and registers to an interleaving multithreading mode” on lines 18-19 on p.17 of the instant application. It is unclear what mode the processor was in prior to being “returned” into interleaving mode. Please correct the claim language to more clearly define the metes and bounds of the claim.

10. Regarding claim 7, the limitation, “a bus coupling the multimedia multithreading processor” is stated on line 16 of p.16 of the instant application. It is unclear what this bus

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couples with the processor, as it is not claimed to be coupling anything else. Please correct the claim language to more clearly point out how the bus relates to the invention as claimed. See a similar problem in claim 17.

11. Regarding claim 7, the claim language recites the limitation "the multimedia multithreading processor" in line 16 of p.16 of the instant application. There is insufficient antecedent basis for this limitation in the claim. For the purposes of this examination, the Examiner will assume that "the multimedia multithreading processor" is the "mixed-mode multithreading processor" claimed on line 15 of p.16. Please see similar problems in claim 13 and claim 17.

Claim Rejections - 35 USC § 102

12. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

13. Claims 1-12 and 14-19 are rejected under 35 U.S.C. 102(b) as being anticipated by Parady, U.S. Patent No. 5,933,627.

14. Regarding claims 1 and 7, taking claim 7 as exemplary, Parady has taught a data processing system, comprising:

- a. A memory unit (see "To Main Memory" of Fig.2 and 178 of Figs. 5/6),
- b. A mixed-mode multithreading processor (see Fig.3),

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- c. A bus coupling the multimedia multithreading processor (see 182 of Figs.5/6 and Col.5 lines18-23),
 - d. Wherein the multimedia multithreading processor comprises:
 - I. A thread control unit (112 of Fig.3),
 - II. A multithreaded register file having a plurality of registers (48, 50 of Fig.3),
 - III. A plurality of hold latches (110 of Fig.3),
 - IV. Wherein each of a plurality of the registers in the multithreaded register file and each of a plurality of the hold latches stores data representing a first instruction thread and a second instruction thread (see Col.3 lines 44-55),
 - V. The thread control unit provides thread control signals to said hold latches and registers selecting a thread using said data (see Fig.3 and Col.3 lines 44-55).
15. Claim 1 is nearly identical to claim 7, differing in its lack of a memory unit and a bus, but encompassing the same scope as claim 7. Therefore, claim 1 is rejected for the same reasons as claim 7.
16. Regarding claims 2 and 8, taking claim 8 as exemplary, Parady has taught the data processing system as recited in claim 7, wherein the thread control unit via the thread control signal places at least one of the plurality of the hold latches and at least one of the plurality of the registers into an interleaving multithreading mode (see Col.4 lines 18-29).

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17. Claim 2 is nearly identical to claim 8, differing in its parent claim, but encompassing the same scope as claim 8. Therefore, claim 2 is rejected for the same reasons as claim 8.

18. Regarding claims 3 and 9, taking claim 9 as exemplary, Parady has taught the data processing system as recited in claim 7, wherein the thread control unit, responsive to a determination that a latency in an instruction exceeding a first predetermined time has occurred in one of the two threads, sends control signals to said hold latches and register for reading out data exclusively from the other of the two threads until a second predetermined time has elapsed (see Col.2 lines 18-24 and Col.4 lines 42-52). Here, a L2 cache miss has been predetermined to have a “long latency”, and causes a thread switch from the thread executing the long latency operation (see Col. 3 lines 57-65), which causes data to be read only from the registers associated with that thread (see Col.3 lines 44-55). Furthermore, a second embodiment uses a round-robin counter to count to a predetermined value (which equates to a predetermined time period) before signaling a thread switch see Col.4 lines 9-12).

19. Claim 3 is nearly identical to claim 9, differing in its parent claim, but encompassing the same scope as claim 9. Therefore, claim 3 is rejected for the same reasons as claim 9.

20. Regarding claims 4 and 10, taking claim 10 as exemplary, Parady has taught the data processing system as recited in claim 9, wherein the thread control unit returns said hold latches and registers to an interleaving multithreading mode after the expiration of the second time period (see Col.4 lines 8-30 and 42-52). Here, after the thread which had the “long latency” memory operation and subsequent thread switch is completed, round-robin (among other) interleaving mode can be resumed (see Col. 4 lines 42-52).

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21. Claim 4 is nearly identical to claim 10, differing in its parent claim, but encompassing the same scope as claim 10. Therefore, claim 4 is rejected for the same reasons as claim 10.

22. Regarding claims 5 and 11, taking claim 11 as exemplary, Parady has taught the data processing system as recited in claim 9, wherein the latency in an instruction exceeding a first predetermined time results from a load instruction that misses in a data cache (see Col.3 lines 57-65).

23. Claim 5 is nearly identical to claim 11, differing in its parent claim, but encompassing the same scope as claim 11. Therefore, claim 5 is rejected for the same reasons as claim 11.

24. Regarding claims 6 and 12, taking claim 12 as exemplary, Parady has taught the data processing system as recited in claim 9, wherein the latency in an instruction exceeding a first predetermined time results from a mispredicted branch (see Col.4 lines 5-8).

25. Claim 6 is nearly identical to claim 12, differing in its parent claim, but encompassing the same scope as claim 12. Therefore, claim 6 is rejected for the same reasons as claim 12.

26. Regarding claims 14 and 17, taking claim 17 as exemplary, Parady has a data processing system, comprising:

- a. A memory unit (see "To Main Memory" of Fig.2 and 178 of Figs. 5/6),
- b. A mixed-mode multithreading processor (see Fig.3),
- c. A bus coupling the multimedia multithreading processor (see 182 of Figs.5/6 and Col.5 lines18-23),
- d. Wherein the multimedia multithreading processor comprises:
 - I. A plurality of flow through latches (48, 50 of Fig.3),
 - II. A plurality of hold state latches (110 of Fig.3),

III. Wherein the hold state latches store two data units, with one data unit corresponding to a first thread and a second data unit corresponding to a second thread (see entry for “Thread 0” and “Thread 1” in 110 of Fig.3, and Col.3 lines 49-55),

IV. Control signals determine which of the two data units is read out of each of the plurality of hold state latches (see Col.3 lines 49-55).

27. Claim 14 is nearly identical to claim 17, differing in its lack of a memory unit and a bus, but encompassing the same scope as claim 17. Therefore, claim 14 is rejected for the same reasons as claim 17.

28. Regarding claims 15 and 18, taking claim 18 as exemplary, Parady has taught the data processing system as recited in claim 17, wherein, responsive to a determination that one thread is not active, reading data corresponding to only one of the threads for a period of time (see Col.2 lines 19-20, Col.3 lines 57-65 and Col.4 lines 42-46). Here, the thread switch occurs when there is a long-latency memory operation, which causes the thread executing the operation to be temporarily inactive (see Col.2 lines 18-20 and Col.3 lines 57-65). A new thread is then operated on until it is switched out of (see Col.4 lines 42-46).

29. Claim 15 is nearly identical to claim 18, differing in its parent claim, but encompassing the same scope as claim 18. Therefore, claim 15 is rejected for the same reasons as claim 18.

30. Regarding claims 16 and 19, taking claim 19 as exemplary, Parady has taught the data processing system as recited in claim 18, wherein the period of time is a predetermined amount of time corresponding to a predicted latency in the one thread that is not active (see Col.2 lines 18-24). Here, a L2 cache miss has been predetermined to have a “long latency”, and causes a

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thread switch from the thread executing the long latency operation (see Col. 3 lines 57-65).

Furthermore, a second embodiment uses a round-robin counter to count to a predetermined value (which equates to a predetermined time period) before signaling a thread switch (see Col.4 lines 9-12).

31. Claim 16 is nearly identical to claim 19, differing in its parent claim, but encompassing the same scope as claim 19. Therefore, claim 16 is rejected for the same reasons as claim 19.

Claim Rejections - 35 USC § 103

32. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

33. Claim 13 is rejected under 35 U.S.C. 103(a) as being unpatentable over Parady, U.S.

Patent No. 5,933,627 as applied to claim 7 above, and further in view of Patterson et al.,

Computer Organization & Design: The Hardware/Software Interface (hereinafter Patterson).

34. Regarding claim 13, Parady has taught the data processing system as recited in claim 7, wherein the multimedia multithreading processor is a first multimedia multithreading processor, the thread control unit is a first thread control unit, the hold latches are first hold latches, the multithreaded register file is a first multithreaded register file, the plurality of registers are a plurality of first registers, and the data is a first data (see above paragraphs 14-15).

35. Parady has not explicitly taught wherein the processor further comprises:

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- a. A second multimedia multithreading processor, wherein the second multimedia multithreading processor comprises:
 - I. A second thread control unit,
 - II. A second multithreaded register file having a plurality of second registers,
 - III. A plurality of second hold latches,
 - IV. Wherein each of a plurality of the second register s and each of a plurality of the second hold latches stores second data representing a third instruction thread and a fourth instruction thread, and
 - V. The second thread control unit provides second thread control signals to said second hold latches and second registers selecting a thread using said second data.

36. However, Patterson has taught that having multiple processors provides redundancy and fault tolerance, as well as the higher performance than a single processor (see p.712). Therefore, one of ordinary skill in the art would have found it obvious to modify the processor of Parady by adding a second processor, identical to the first, in order to provide redundancy and improve performance.

37. Furthermore, while a Parady has taught a single processor comprising all of the limitations of claim 7 (see above paragraphs 14-15), Parady has not taught a second processor comprising those same limitations. However, the inclusion of a second processor with no reference in the claims as to how it is configured in relation to the first process provides no new or unexpected result over the prior art of record. Therefore, one of ordinary skill in the art would have found it obvious to duplicate the processor, creating a second processor comprising all of

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the limitations of the first processor of Parady (see *In re Harza*, 274 F.2d 669, 671, 124 USPQ 378, 380 (CCPA 1960)).

Conclusion

38. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Applicant is reminded that in amending in response to a rejection of claims, the patentable novelty must be clearly shown in view of the state of the art disclosed by the references cited and the objections made. Applicant must also show how the amendments avoid such references and objections. See 37 CFR § 1.111(c).

39. Chesson et al., U.S. Patent No. 5,524,250, has taught a processor for executing threads with each thread having its own set of registers.

40. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Barry J. O'Brien whose telephone number is (703) 305-5864.

The examiner can normally be reached on Mon.-Fri. 6:30am-4:00pm.


If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (703) 305-9712. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

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41. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Barry J. O'Brien
Examiner
Art Unit 2183

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4/2/2004



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